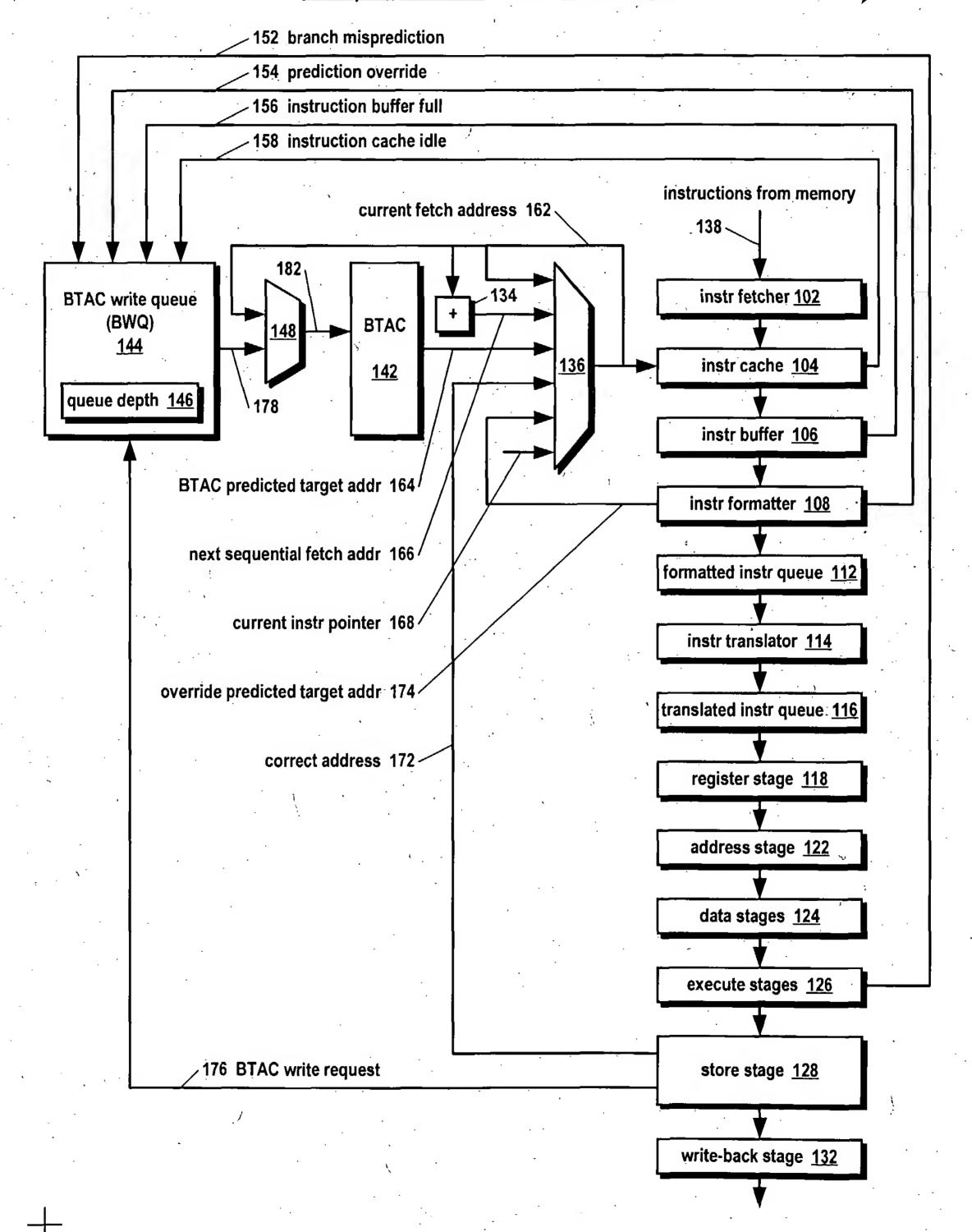
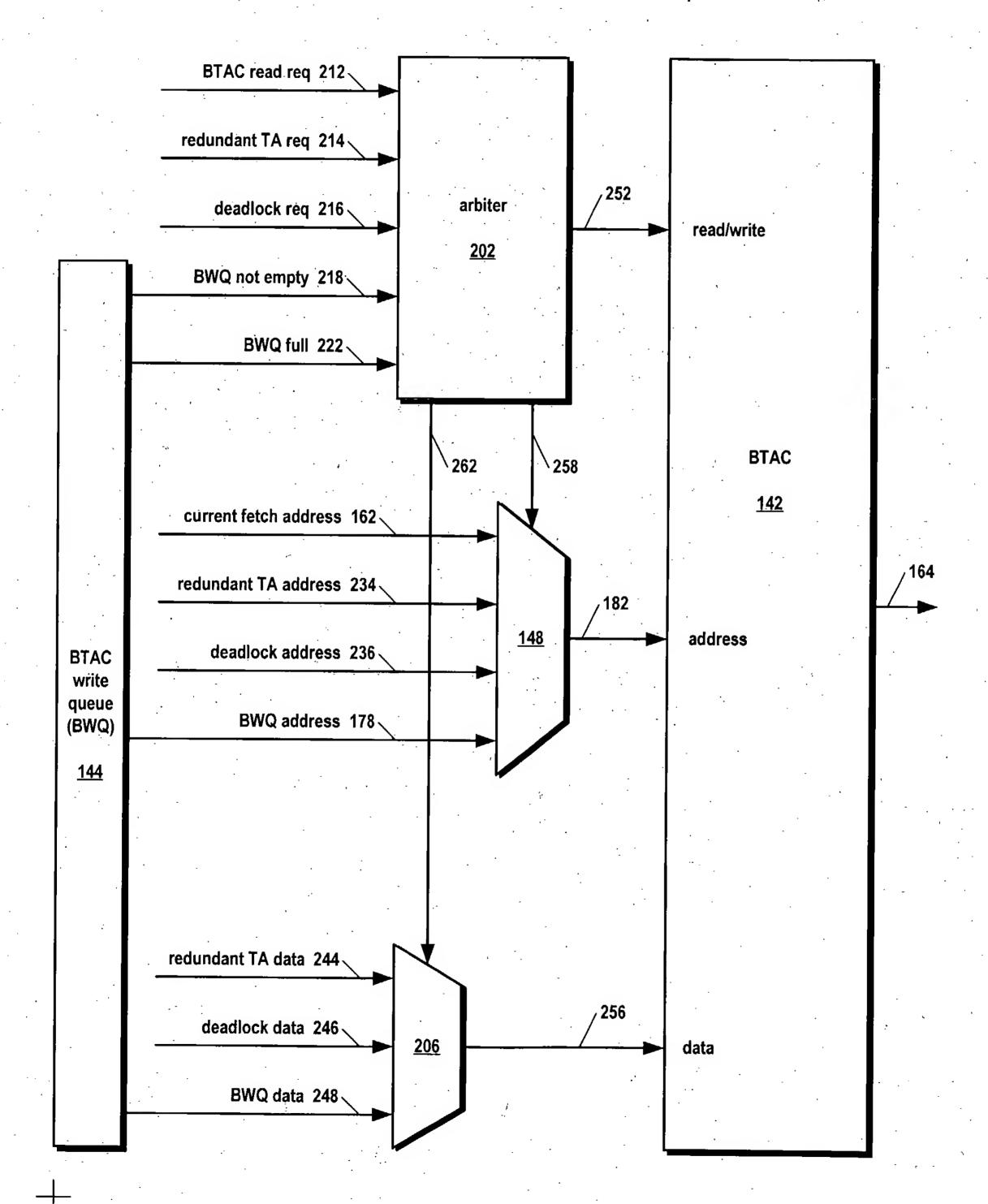
### Microprocessor with BTAC Write Queue

**-- 10**0

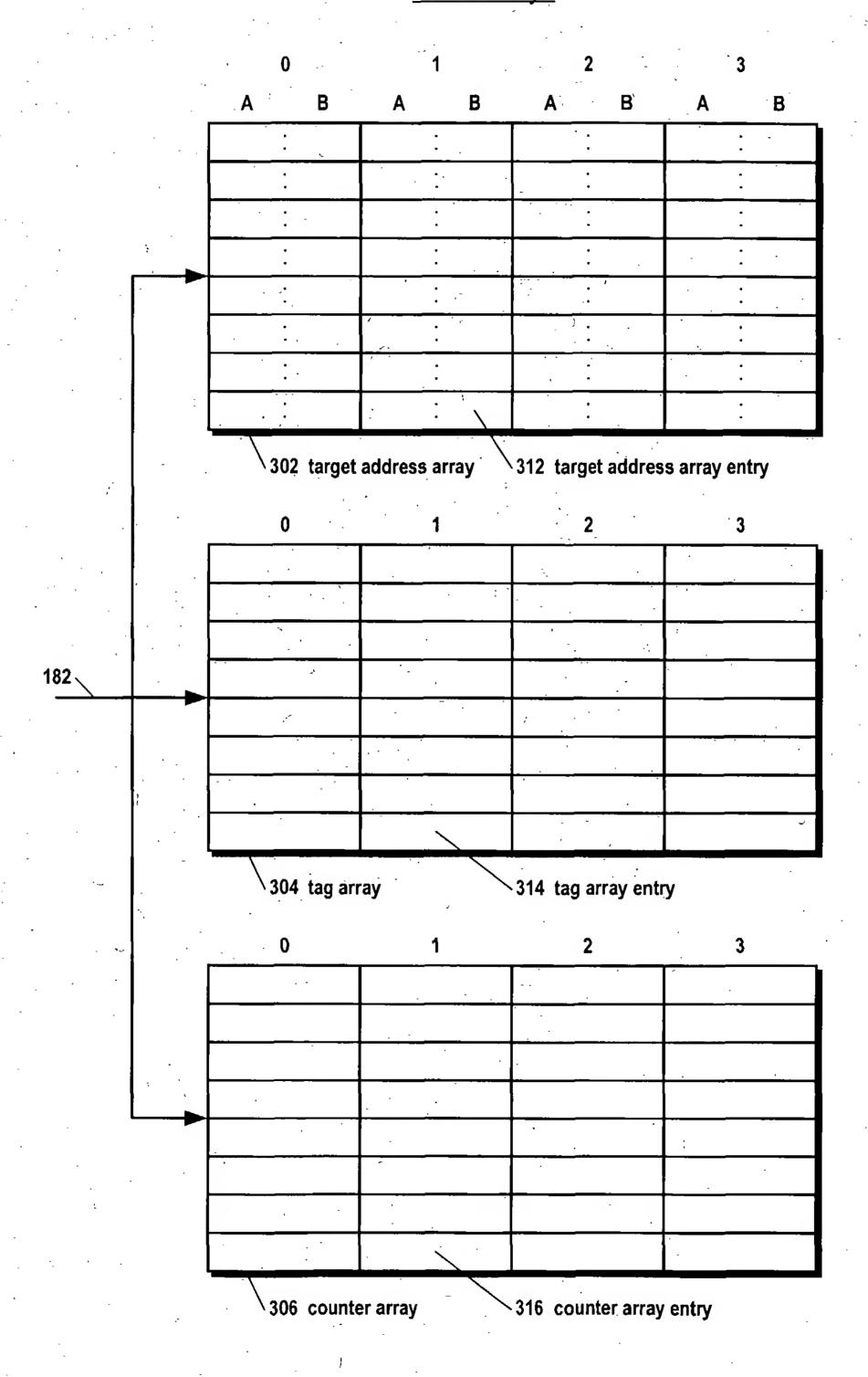


# Microprocessor with BTAC Write Queue





# BTAC Arrays



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Fig. 4

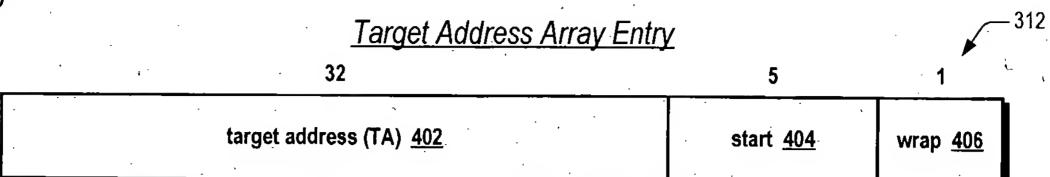


Fig. 5

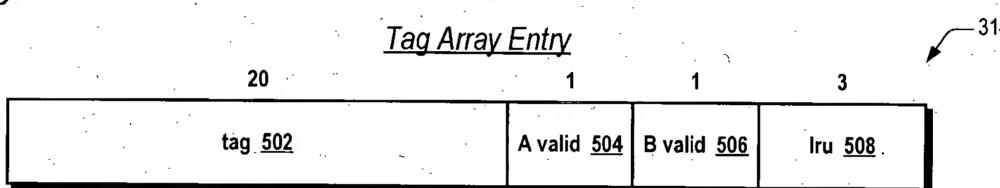


Fig. 6

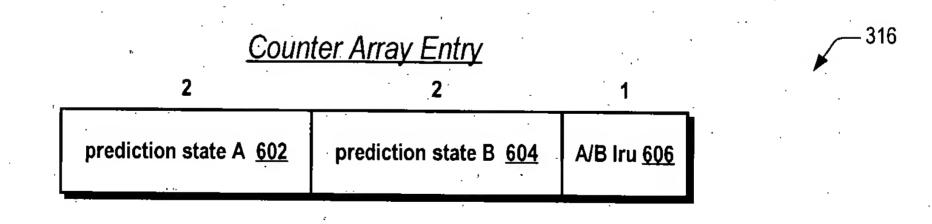


Fig. 7

,0	BTAC Write Request								176		
_	32	32	5	. 1	. 1	1	1	1	4		
	branch instr addr <u>702</u>	target address (TA) <u>706</u>	start 708	wrap 712	we-A 714	we-B 716	inv-A 718	inv-B 722	way <u>724</u>		

## BTAC Write Queue

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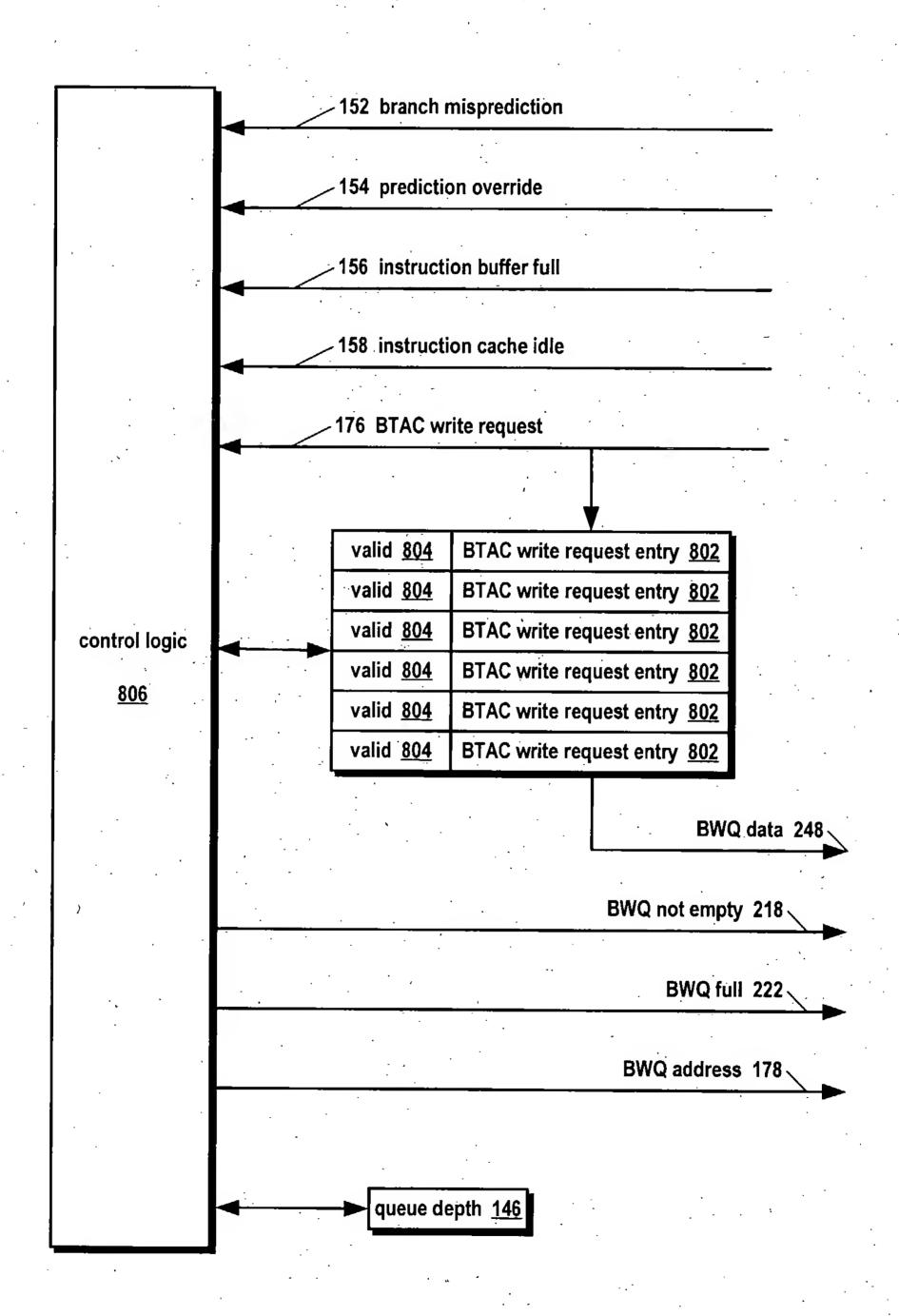
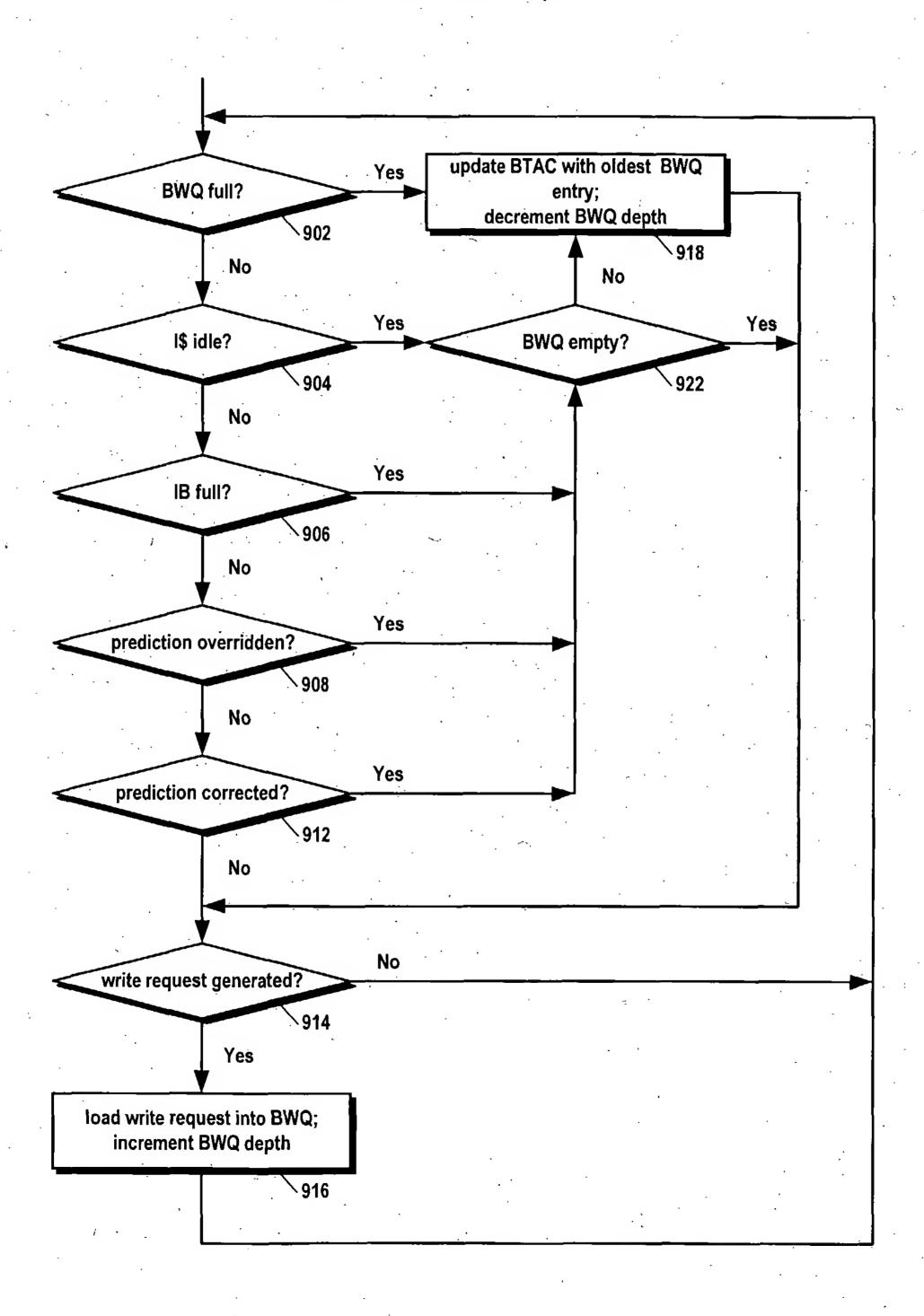
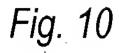
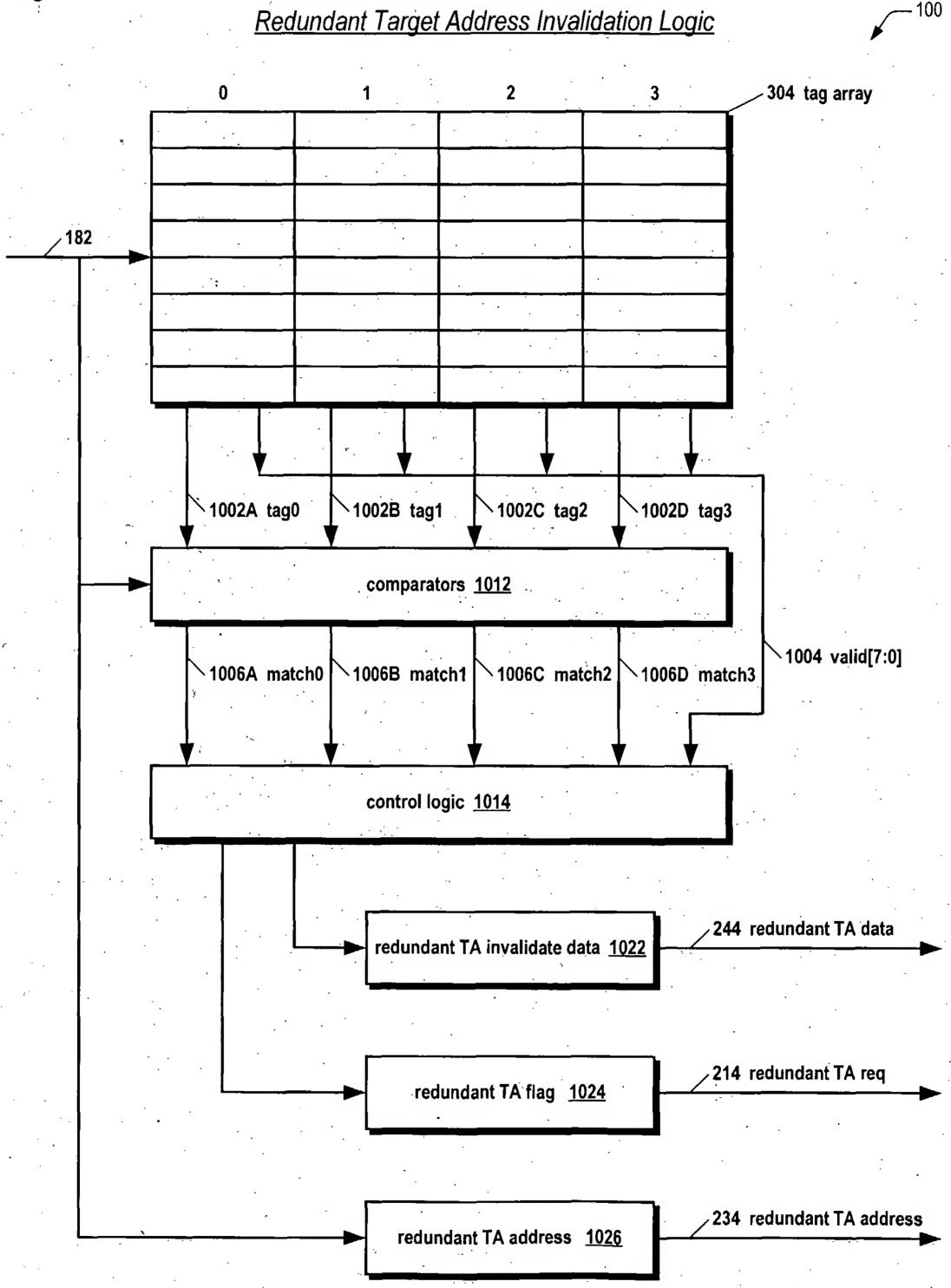


Fig. 9

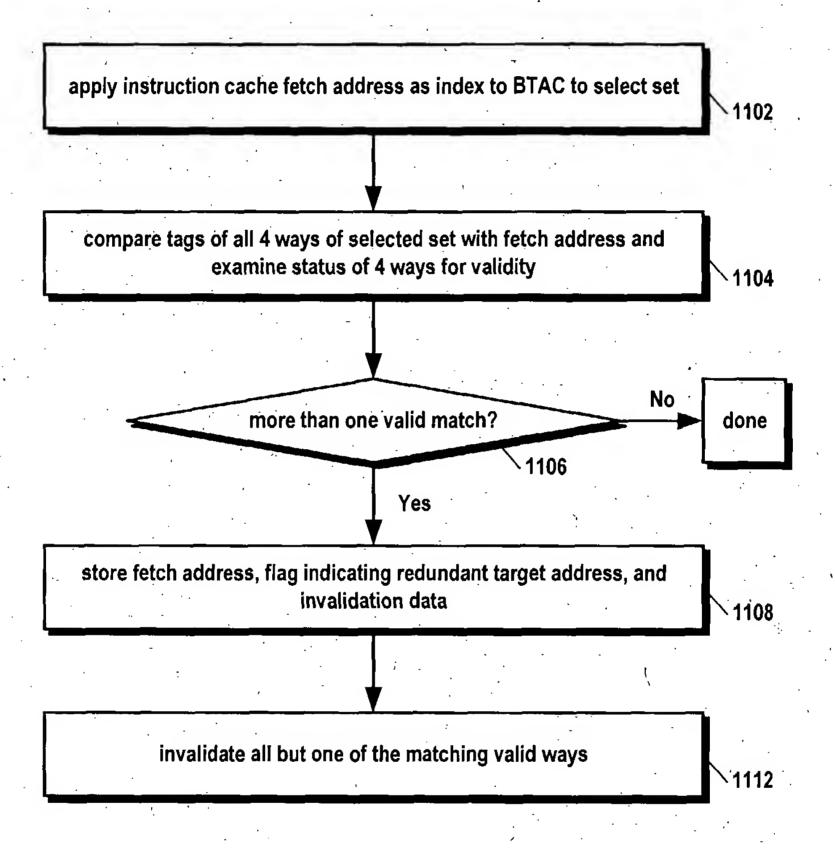
## BTAC Write Queue Operation

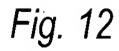






### Redundant Target Address Invalidation Operation





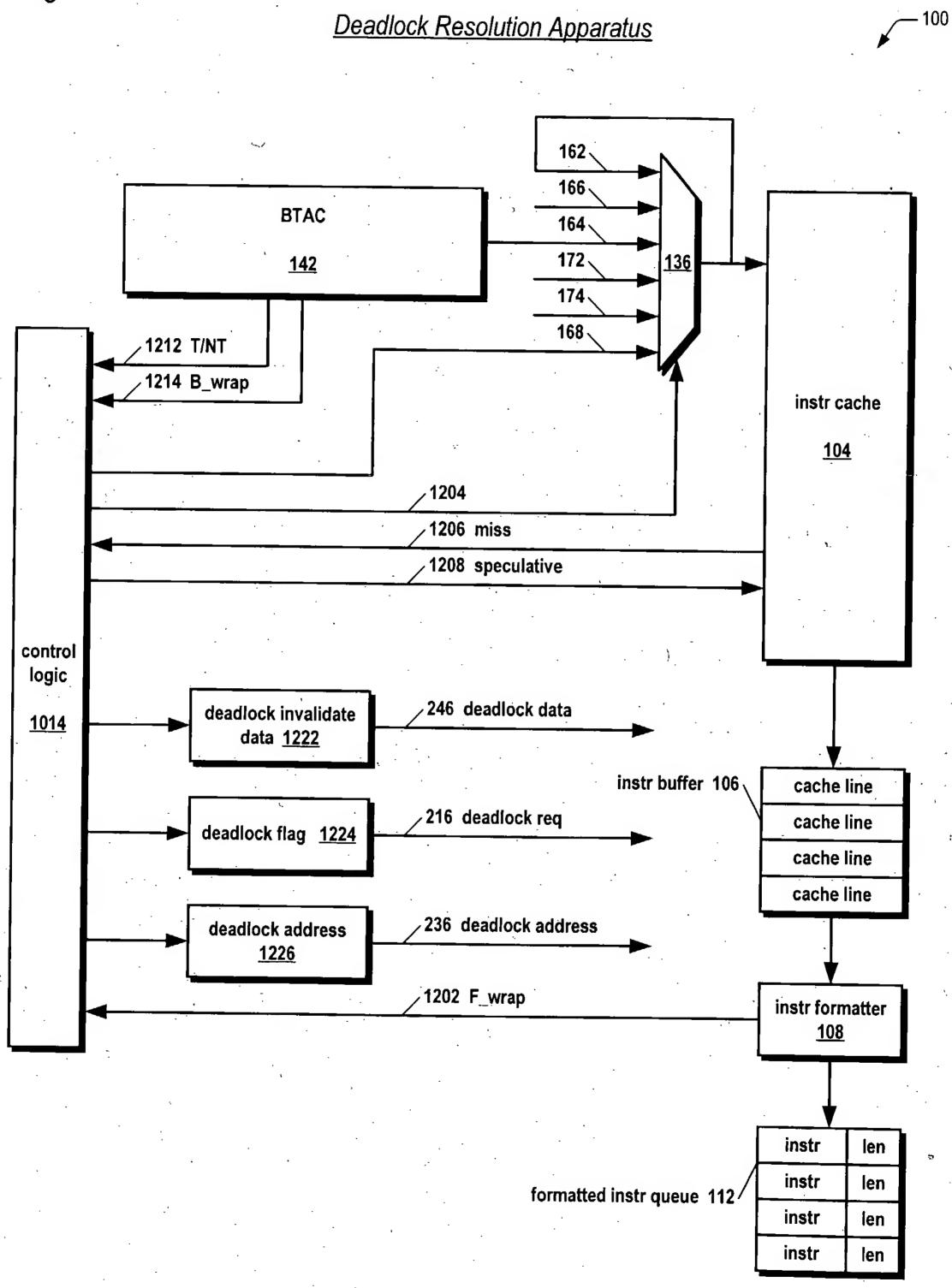


Fig. 13

#### Deadlock Resolution Apparatus Operation

